7 Key Relationships of Electrical Harmonics You Should Understand

Michael A McGraw: Harmonic Consultant Five Star Electric

There are seven key relationships that will provide understanding of the consequences of electrical harmonics within a distribution system, and existing distribution system conditions that complicate harmonic mitigation within any given grid.

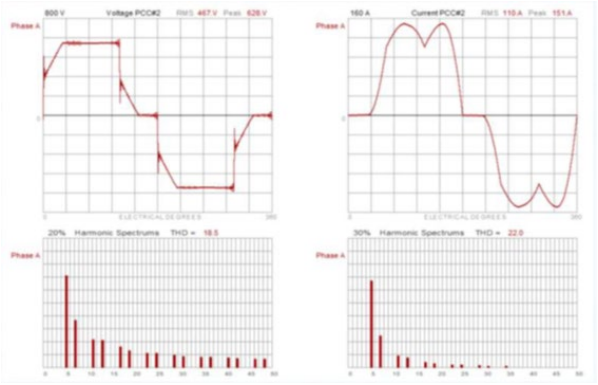
Within each topic, I will reference back to either a published white paper or IEEE published paper which I either co-authored or contributed to, for a more in-depth discussion. The discussions are forwarded to augment your systemic strategies when facing a harmonic circuit challenge.

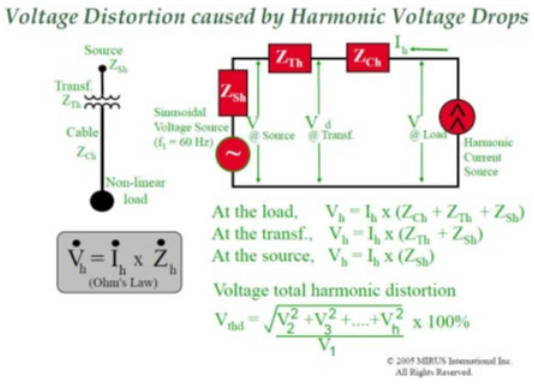
- ***SYSTEM IMPEDANCE/SOURCE AVAILABLE SHORT CIRCUIT & THE RELATIONSHIP BETWEEN CURRENT HARMONIC AND ASSOCIATED VOLTAGE DISTORTION.***
- ***SOURCE VOLTAGE DISTORTION AND THE CREATION OF CURRENT HARMONIC FROM LINEAR LOADS***
- ***SYSTEMIC VOLTAGE IMBALANCES WILL COMPLICATE YOUR HARMONIC CONDITION***
- ***HOW VOLTAGE DISTORTION CAN CREATE DC CONTROL RIPPLE AND COMPROMISE ELECTRONIC EQUIPMENT***
- ***UTILIZATION OF IGBT SWITCHING IS NOT A CURE FOR YOUR HARMONIC CONDITION, BUT IT DOES PROVIDE A MEASURE OF LOWER FREQUENCY CURRENT HARMONIC MITIGATION. THESE HARMONIC STRATEGIES WILL INJECT SUPRAHARMONICS INTO YOUR CIRCUIT.***
- ***TRUE/TOTAL POWER AND EFFICIENCY IS A FUNCTION OF THE HARMONIC REACTIVE POWER WITHIN ANY GIVEN CIRCUIT***
- ***ELECTRICAL HARMONICS WITHIN A CIRCUIT CAN TRIGGER RESONANCE/RINGING VOLTAGE DISTURBANCES, WHICH CAN COMPROMISE DISTRIBUTION AND GRID INTEGRITY***

SYSTEM IMPEDANCE/SOURCE AVAILABLE SHORT CIRCUIT & THE RELATIONSHIP BETWEEN CURRENT HARMONIC AND ASSOCIATED VOLTAGE DISTORTION

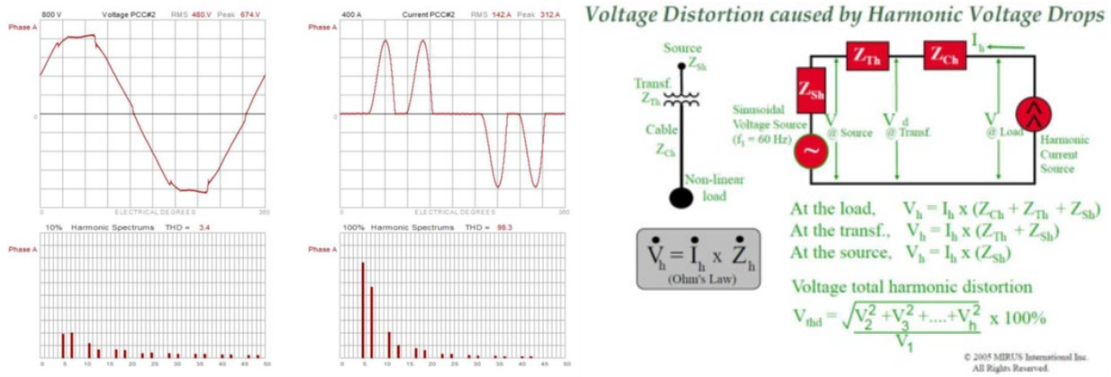
Nonlinear loads draw current in a non-sinusoidal manner, where the fundamental 60 Hz Frequency is impacted by higher frequency current draws from the switching frequency of the rectifier segment of the load device. Typically, we associate this with ASD/VFD applications, but it will exist in Diode Bridge or IGBT rectifier loads, UPS, DC rectifiers, and inductive heating systems.

The current characteristic then impacts the system voltage regulation, i.e. the instantaneous change in current negative and positive (di/dt) will create a corresponding change in the system voltage rate of change (dv/dt) of the source. The injection of the current harmonic into the system impedance creates voltage distortion.





The lower the Available Short Circuit Current of the Source: The lower the regulation of the source, i.e., the weaker the source. Any given current harmonic injection will have a lower calculated Ithd but a greater impact on the associated Vthd. The weaker the system the greater the Vthd (Total Harmonic Distortion – Vthd) and the lower the Ithd (Total Harmonic Distortion – Current)



The greater the Available Short Circuit of the Source: The tighter the regulation of the source, i.e., the stiffer the source. Any given current harmonic injection will have a higher calculated Ithd but a lower impact on the associated Vthd.

This is why per IEEE519 Harmonic Recommendations, you are allowed a higher Current Harmonic Demand Distortion as the short circuit ratio at the Point of Common Coupling increases… reference Table 2 & 3, IEEE519-2022, Page 18 & 20, Section 5.3 & 5.4 Current distortion limits for systems nominally rated 120 V through 69 Kv & above 69 Kv through 161 Kv:

Table 2—Current distortion limits for systems rated 120 V through 69 kV

Maximum harmonic current distortion in percent of I_L						
Individual harmonic order[b]						
I_{SC}/I_L	$2 \le h < 11$[a]	$11 \le h < 17$	$17 \le h < 23$	$23 \le h < 35$	$35 \le h \le 50$	TDD
<20[c]	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

[a] For $h \le 6$, even harmonics are limited to 50% of the harmonic limits shown in the table.

[b] Current distortions that result in a dc offset, e.g., half-wave converters, are not allowed.

[c] Power generation facilities are limited to these values of current distortion, regardless of actual I_{SC}/I_L unless covered by other standards with applicable scope.
where:
I_{SC} = maximum short-circuit current at PCC
I_L = maximum demand load current at PCC under normal load operating conditions

Table 3—Current distortion limits for systems rated above 69 kV through 161 kV

Maximum harmonic current distortion in percent of I_L						
Individual harmonic order[b]						
I_{SC}/I_L	$2 \le h < 11$[a]	$11 \le h < 17$	$17 \le h < 23$	$23 \le h < 35$	$35 \le h \le 50$	TDD
<20[c]	2.0	1.0	0.75	0.3	0.15	2.5
20<50	3.5	1.75	1.25	0.5	0.25	4.0
50<100	5.0	2.25	2.0	0.75	0.35	6.0
100<1000	6.0	2.75	2.5	1.0	0.5	7.5
>1000	7.5	3.5	3.0	1.25	0.7	10.0

[a] For $h \le 6$, even harmonics are limited to 50% of the harmonic limits shown in the table.

[b] Current distortions that result in a dc offset, e.g., half-wave converters, are not allowed.

[c] Power generation facilities are limited to these values of current distortion, regardless of actual I_{SC}/I_L unless covered by other standards with applicable scope.
where
I_{SC} = maximum short-circuit current at PCC
I_L = maximum demand load current at PCC under normal load operating conditions

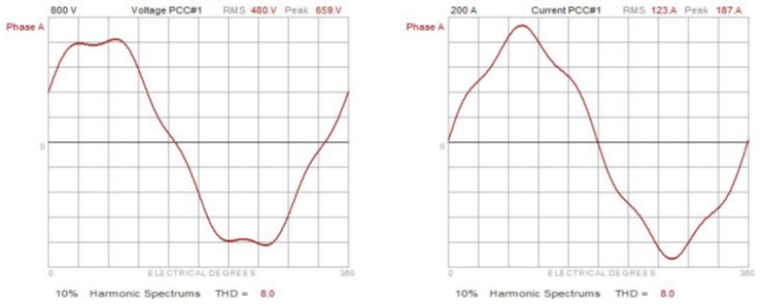
Theoretically, by controlling the levels of current harmonics within any given circuit, you can control the amount of induced voltage distortion created assuming no Source/Background Voltage Distortion, Systemic Voltage Imbalance and/or no Systemic Resonance within the circuit due to uncontrolled reactive power sources/load structures.

- An 'Intuitive Understanding' of Electrical Harmonics: A Conversation
- Electrical Harmonics 101: An Overview of the Fundamentals of Electrical Harmonics and Discussion of Mitigation Strategies.
- An Intuitive Understanding of Electrical Harmonics FSE-MM-2026

SOURCE VOLTAGE DISTORTION AND THE CREATION OF CURRENT HARMONIC FROM LINEAR LOADS

Any Linear Load Structure fed by a Distorted Source Voltage will run less efficiently and draw current in a non-linear fashion, i.e., will now behave electrically as a non-linear load. This must be understood that any harmonic study must have the capability to inject Source or Systemic Voltage Distortion into all the load structures to create an accurate projection of PCC (Point of Common Coupling) current harmonic condition.

Below is a graphic of a linear load being fed by a source which exhibits a wave trace from a 100kW linear load being fed from an IEEE 519-2022 compliant 8% Vthd system.

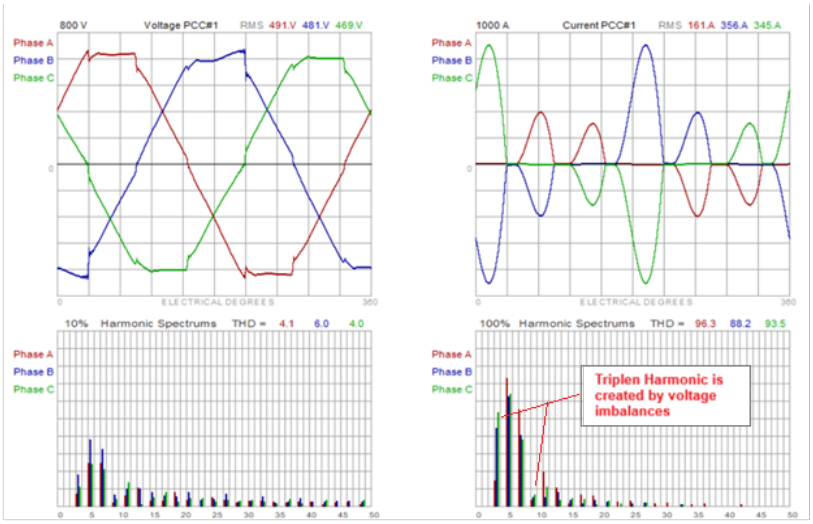


Generally, the level of current harmonic generated by the voltage distortion will be the same percentage of fundamental when measured at the input of the associated linear load device.

SYSTEMIC VOLTAGE IMBALANCES WILL COMPLICATE YOUR HARMONIC CONDITION

The greater the source voltage imbalance being provided to a non-linear load, the greater the impact to Current Harmonic (Ithd) and associated Voltage Distortion (Vthd) experienced. The system Imbalances can be created by either Utility or other Potential Sources and/or unbalanced single-phase loads within the associated load circuit.

Harmonic #	V L-L %fund	V L-L rms	I L %fund	I L rms
1	100.00	490.79	100.00	116.10
2	0.00	0.00	0.01	0.01
3	0.71	3.51	14.91	17.31
4	0.00	0.00	0.00	0.00
5	2.49	12.22	73.34	85.14
6	0.00	0.00	0.01	0.01
7	2.47	12.14	55.00	63.86
8	0.00	0.00	0.00	0.00
9	0.25	1.21	3.68	4.28
10	0.00	0.00	0.00	0.00
11	0.62	3.07	19.57	22.72
12	0.00	0.00	0.00	0.00
13	1.09	5.34	10.88	12.63
14	0.00	0.00	0.00	0.00
15	0.32	1.57	1.98	2.30
16	0.00	0.00	0.00	0.00
17	0.30	1.47	6.92	8.03
18	0.00	0.00	0.00	0.00
19	0.80	3.95	6.48	7.52
20	0.00	0.00	0.00	0.00
21	0.37	1.82	0.98	1.13
22	0.00	0.00	0.00	0.00
23	0.08	0.39	2.64	3.07
24	0.00	0.00	0.00	0.00
25	0.53	2.61	3.38	3.93
26	0.00	0.00	0.00	0.00
27	0.38	1.87	0.69	0.81
28	0.00	0.00	0.00	0.00
29	0.23	1.15	1.92	2.23
30	0.00	0.00	0.00	0.00
31	0.32	1.59	2.09	2.43
32	0.00	0.00	0.00	0.00
33	0.35	1.70	0.67	0.78
34	0.00	0.00	0.00	0.00
35	0.29	1.40	1.32	1.53
36	0.00	0.00	0.00	0.00
37	0.20	1.00	1.62	1.88
38	0.00	0.00	0.00	0.00
39	0.29	1.43	0.52	0.60
40	0.00	0.00	0.00	0.00
41	0.28	1.37	0.72	0.84
42	0.00	0.00	0.00	0.00
43	0.12	0.61	1.21	1.40
44	0.00	0.00	0.00	0.00
45	0.25	1.21	0.38	0.44
46	0.00	0.00	0.00	0.00
47	0.28	1.36	0.51	0.59
48	0.00	0.00	0.00	0.00
49	0.10	0.50	0.91	1.05
50	0.00	0.00	0.00	0.00

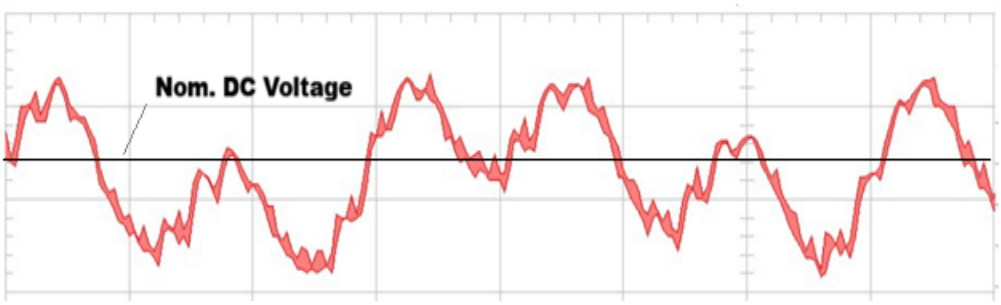


Triplen Harmonics are created when a unbalanced source voltage is feed to a non-linear load. This can then create complications to the associated voltage distortion depending on the regulation of the potential source.

Note that a typical harmonic spectrum from an unbalanced source will have elevated levels of triplen harmonics, i.e. 3rd and 9th typically, which can create non-typical current within the neutral bond upstream of the non-linear load.

- Comparative of VFD Drive, Harmonic Mitigation Methodology, and Output PQ Options A Practical Discussion and Concept Overview
- An Intuitive Understanding of Electrical Harmonics FSE-MM-2026

HOW VOLTAGE DISTORTION CAN CREATE DC CONTROL RIPPLE AND COMPROMISE ELECTRONIC EQUIPMENT

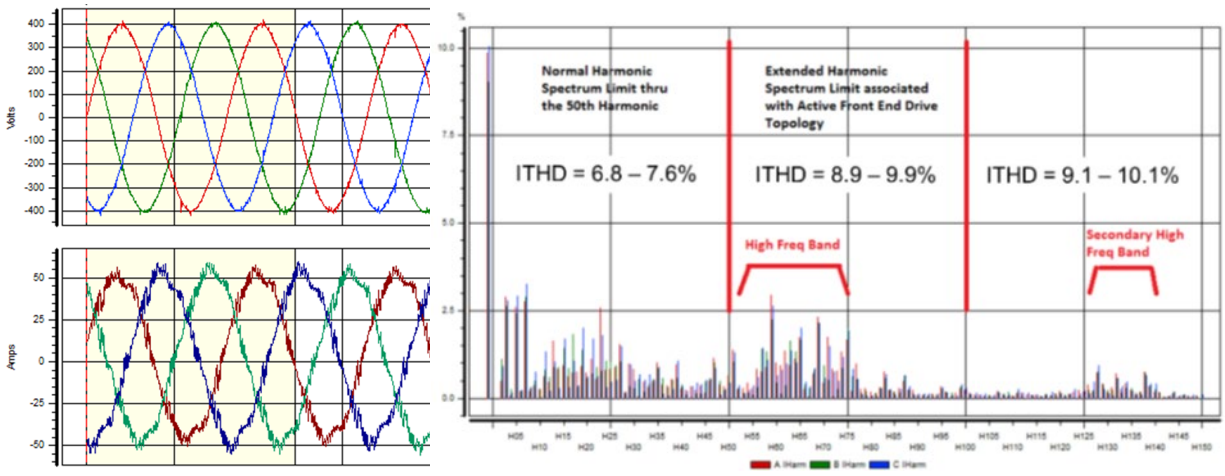


A distorted voltage (Vthd) supplying a DC Power Supply can create additional DC bus ripple/distortion above the nominal amount, which has a significant impact on all control equipment being supplied by that DC source. The image shows the effects of low and higher frequency voltage distortion on an AC – DC power supply. This can then create issues for the LV DC components, sensors and transducers effected.

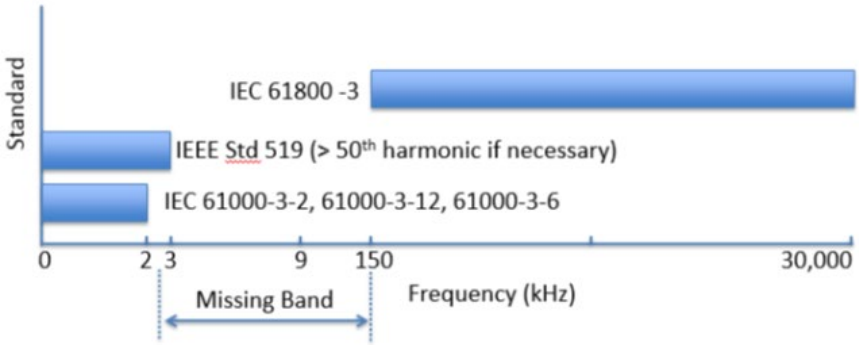
The above wave trace and graphic is an illustration used as an example only of potential DC bus ripple. Typically, the injected DC bus ripple frequency will approximately match the Source Vthd frequency characteristic and frequency. A key element of controlling systemic voltage distortion via current harmonic mitigation is to minimize the DC bus ripple within the control circuits and with VFD DC bus assemblies in order to avoid nuisance voltage related trips and damage to DC bus ripple control capacitor assemblies.

UTILIZATION OF IGBT SWITCHING IS NOT A CURE FOR YOUR HARMONIC CONDITION, BUT IT DOES PROVIDE A MEASURE OF LOWER FREQUENCY CURRENT HARMONIC MITIGATION. THESE HARMONIC STRATEGIES WILL INJECT SUPRAHARMONICS INTO YOUR CIRCUIT

High speed switching devices, such as IGBT based rectification or inverter applications will create Supraharmonics current characteristics which must be considered and evaluated within a credible harmonic review, modeling program, or testing protocol – typically between 2 kHz and 150 kHz. What you will rarely hear from Active Front End (AFE) VFD manufacturers is that this switching introduces higher frequency harmonics, normally above the 50th. When measurements are taken up to the 50th, current total harmonic distortion (ITHD) is often quite low but when measured up to the 100th or higher, ITHD almost always exceeds their claimed performance levels which consider only harmonics up to the 50th. Manufacturers, therefore, often design active harmonic mitigation equipment that generates relatively high levels of mid-range frequencies, particularly since switching frequencies of IGBTs typically fall precisely within this range. Below is a harmonic spectrum for an AFE drive (IGBT rectified), which shows the higher order harmonic injection typical for this class of equipment.



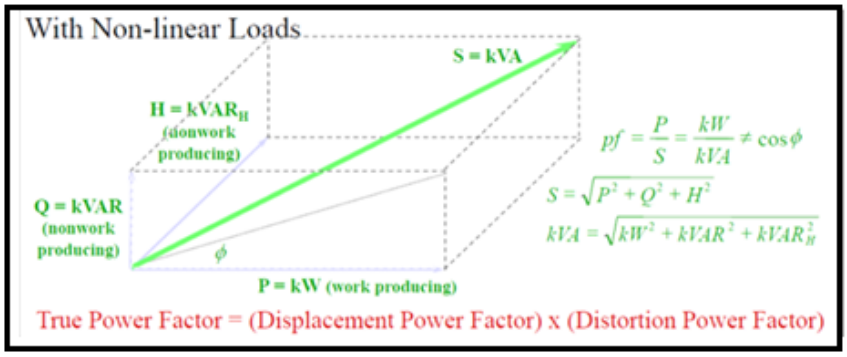
Unfortunately, no IEC or IEEE harmonic performance standards cover specific current harmonic performance standards from 3 kHz – 150 kHz as shown in the below coverage graphic, this is known as the missing bandwidth by some or just the missing band.



I would suggest you review the noted IEEE PCIC paper noted above for a more detailed discussion on this subject. Keep in mind, it does not discuss in detail Active Harmonic Filters. The harmonic frequency distribution is typical whether you are reviewing a AFE VFD or a AHF – Active Harmonic Filter, but the AHF is sized to the harmonic mitigation current versus the actual load current, so the injected consequence of the harmonic is significantly less.

- IEEE/PCIC 2018 Cincinnati OH, Co-Author "Active Harmonic Mitigation – What the Manufacturers Don't Tell You" (PCIC-2018-43) (IEEE Copyrighted Material)

TRUE/TOTAL POWER AND EFFICIENCY IS A FUNCTION OF THE HARMONIC REACTIVE POWER WITHIN ANY GIVEN CIRCUIT



Current Harmonics have a significant impact on the True/Total Power Factor of the Source, considered as non-work producing Harmonic kVAR (Reactive Power).
The key is to understand that even though displacement power factor is measured by most meters, it is not relevant to power factor evaluations anymore, since the most significant source of reactive power consumption within most circuits is now $kVAR_H$ (Harmonic Reactive Power**). KVA is now defined as the root sum squared of the kW, Q and H as noted in the graphic above. Power Factor Surcharges by Utility entities are calculated based on True or Total Power Factor.**

Even though VFD's are listed as being 0.95 pf within most specifications, which is the displacement power factor rating, the tpf (Total/True Power Factor) will be a function of the harmonic reactive power produced and a function of the system impedance noted in in the first section of this discussion. In most cases the True/Total Power Factor will be somewhere between 0.82 and 0.90 contribution from the VFD current harmonic injection into the systemic impedance.

- An 'Intuitive Understanding' of Electrical Harmonics: A Conversation
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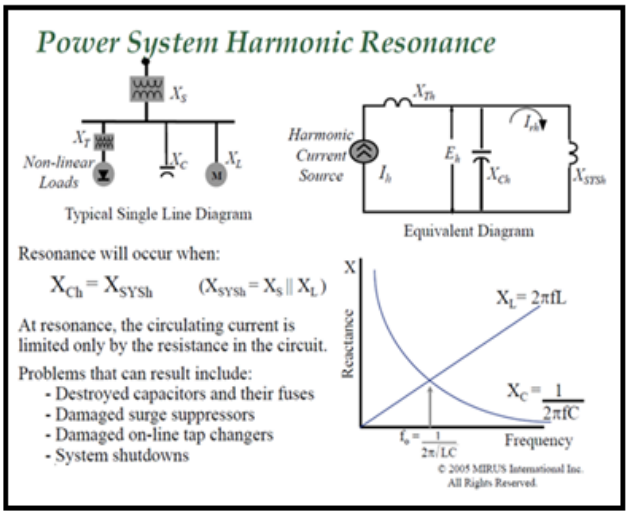
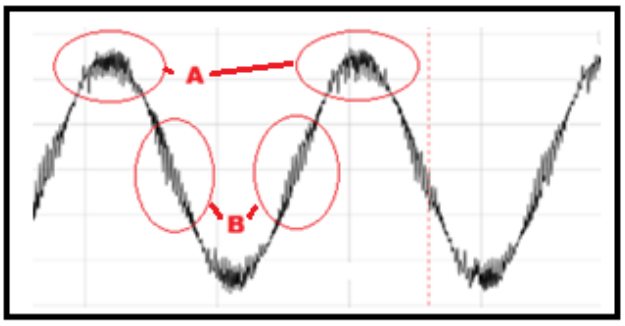
- How Harmonics Have Contributed to Many Power Factor Misconceptions MIRUS-TP003-A

ELECTRICAL HARMONICS WITHIN A CIRCUIT CAN TRIGGER RESONANCE/RINGING VOLTAGE DISTURBANCES, WHICH CAN COMPROMISE DISTRIBUTION AND GRID INTEGRITY

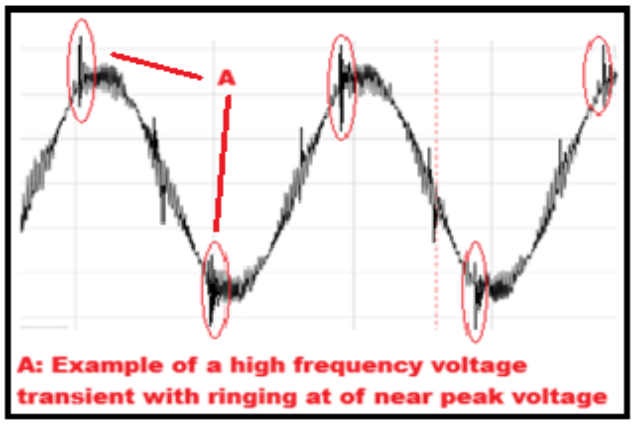


Power systems have a frequency band at which the inductive and capacitive elements are equal. Current harmonic frequencies that are drawn by non-linear loads within this band can result in resonance with the power system. The resonance can present itself in the form of a high frequency general resonance or resonance bank, typically referred to as ringing of the circuit. The resonance or ringing may also display intermittent high voltage transients which will significantly increase dielectric stress on the entire circuit infrastructure. Low frequency resonance, below 3 kHz will elevate the measured Voltage Distortion (Vthd) seen at the "Point of Common Coupling" (PCC) within the circuit making it more difficult to meet the objectives of IEEE519 Table 1 systemic voltage distortion requirements. Below, are three traces with notes of the three noted resonance conditions.



A: Peak Resonance Voltage example
B: Zero Voltage Crossing Resonance example

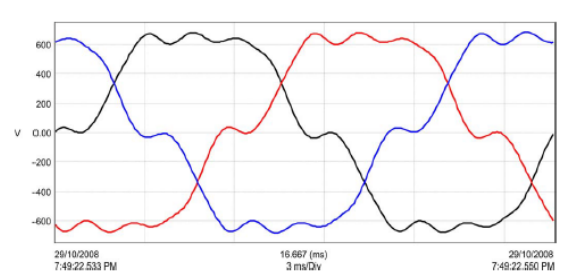
Voltage Reflective Wave (Ringing) and high frequency noise example. Here the resonance is presented at a high frequency (Greater than 3 kHz) from some form of high frequency switching trigger and there is an example of a zero-voltage crossing resonance presenting as well. The trace is presented as an example only. Typical circuit topologies which can create this high frequency noise would be existing upstream power factor correction capacitance (Low Voltage and Medium Voltage), load side Active Front End VFD's where the rectifier IGBT switching frequency is near or at the natural resonance frequency of the circuit, and/or Utility Voltage Correction Capacitance within the upstream circuit.

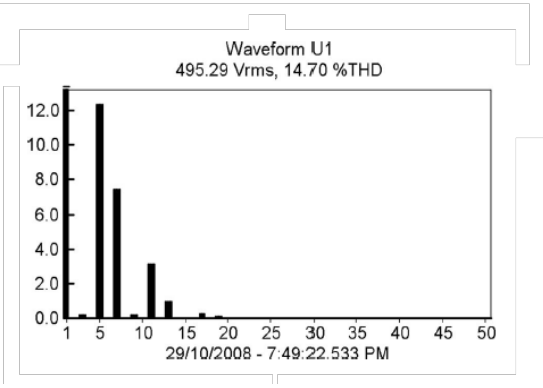


A: Example of a high frequency voltage transient with ringing at of near peak voltage

Intermittent Voltage Transients may present within a resonance wave trace which may be significant and potentially damage the associated circuit and components due to elevated dielectric stress. The graphic has highlighted the transients at or near peak voltage, but it should be noted that these transients and ringing can occur anywhere along the voltage development but typically will be seen at the peak voltage values and in and around zero-voltage crossings, if present. It should be noted that even though the peak voltage of the transient may not be significant indicating a traditional over voltage

condition, the dv/dt of the transient will be the key source of the dielectric stress of the transient to the overall circuit.

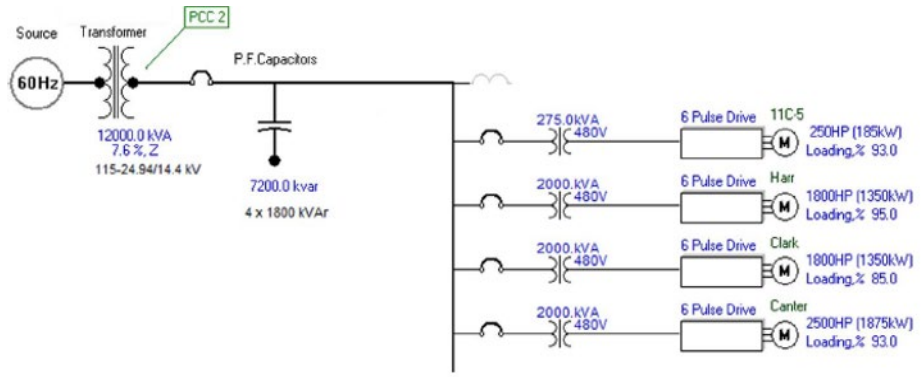




Elevated levels of Source Voltage Distortion (Vthd–bg) can present due to resonance within a Utility source or due to high levels of upstream capacitance reactance within the source infrastructure. *The graphic to the left and above is from a published IEEE paper presented by Mirus International. "Oil Field Retrofit of ESPs to Meet Harmonic Compliance Marek Farbis, Member, IEEE, Anthony H. Hoevenaars, Member, IEEE, and John L. Greenwald.*

Within Section II. "ANALYSIS *A. Power System Resonance with PFC Capacitors:* Adding capacitors in an attempt to improve PF will cause the power system to be tuned to a certain frequency. Parallel resonance occurs when the natural power system inductive reactance matches the capacitive reactance of the capacitors (see Figs. 7–9). When this occurs near the frequency of a predominant harmonic, for example, the 5th, 7th, or 11th, serious consequences can result, …."

This was a real installation, and as can be witnessed, a triplen harmonic (3rd and 9th) is present, and significant 5th, 7th, 11th and 13th, elevating the Vthd within the system to well over 15%. The key here is to understand the source condition and the potential impact of injecting a current harmonic into this resonance circuit and the further deterioration of harmonic condition. With a low frequency resonance condition any harmonic mitigation strategy must be designed so as not to resonate with the source and not attract the systemic voltage distortion which will overload the harmonic mitigation equipment.

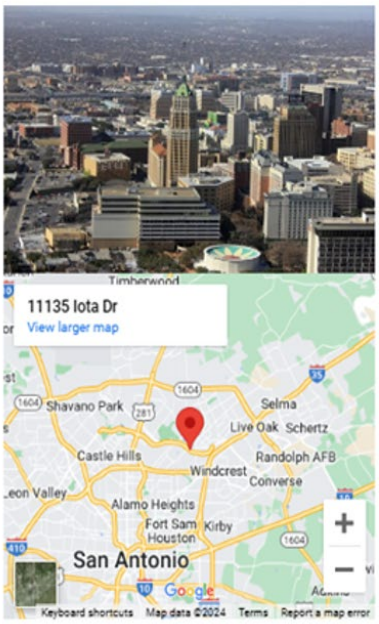


- IEEE/PCIC 2018 Cincinnati OH, Co-Author "Active Harmonic Mitigation – What the Manufacturers Don't Tell You" (PCIC-2018-43) (IEEE Copyrighted Material)

Summary

By understanding these seven relationships, understanding your true harmonic condition and the best strategy to resolve the harmonic challenges; can be achieved. A credible engineering strategy will not only include detail on the associated non-linear load but also the true systemic condition as to the source power quality and a holistic understanding of you load structures, For more information on any of these subjects or if you need assistance with your mitigation strategy, please feel free to contact myself or Five Star directly.

SAN ANTONIO



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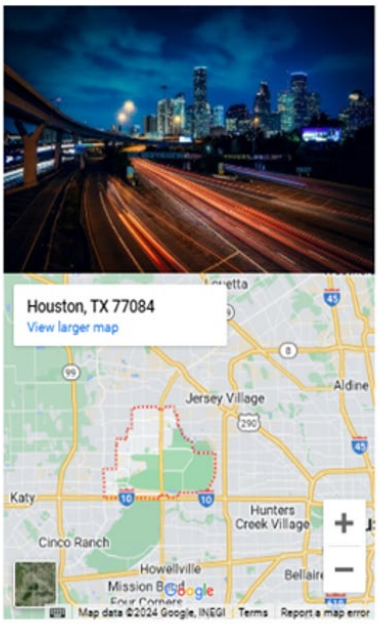

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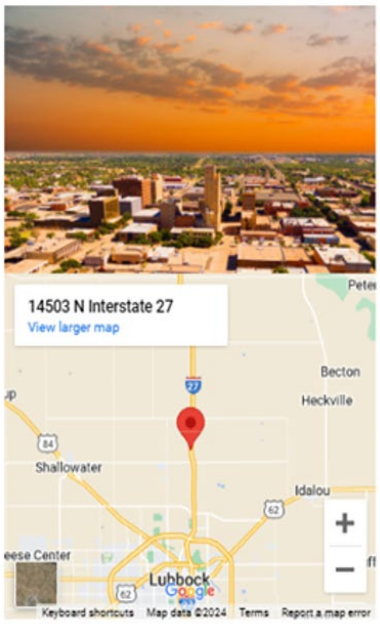

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Mike McGraw - Harmonic Consultant	713-208-8534	mmcgraw@vfd.com

IEEE Reference Materials & Papers: (Copies Available Upon Request)

- IEEE/PCIC 2010 San Antonio TX, Coauthor, "Design Considerations When Applying Various ASD Topologies to Meet Harmonic Compliance" (PCIC-2010-15), ***IEEE/PCIC Third Best Paper 2010 Technical conference Award, San Antonio TX*** (IEEE Copyrighted Material)
- IEEE/PCIC 2018 Cincinnati OH, Co-Author "Active Harmonic Mitigation – What the Manufacturers Don't Tell You" (PCIC-2018-43) (IEEE Copyrighted Material)
- IEEE/PCIC 2025 - 3 Hour Tutorial Primary Author & Presenter: "Harmonic Engineering & Design Challenges for Distribution Circuit and Grid Design"

Mirus International Company White Papers: (Copies Available Upon Request)

- The Need for Harmonic Modeling and Mitigation in Generator Applications: A Conversation and Guide
- An 'Intuitive Understanding' of Electrical Harmonics: A Conversation
- How Harmonics Have Contributed To Many Power Factor Misconceptions MIRUS-TP003-A

Five-Star Electric Presentations & Papers: (Copies Available Upon Request)

- Electrical Harmonics 101: An Overview of the Fundamentals of Electrical Harmonics and Discussion of Mitigation Strategies.
- Electrical Harmonics 102: A Further Review of Electrical Harmonics and Discussion of Mitigation Strategies with Discussion of VFD Secondary Circuit Design Considerations.
- Presentation: Texas Water 2025 Harmonic Mitigation: VFD's & Harmonic Mitigation in Modern Water/Wastewater Applications
- Comparative of VFD Drive, Harmonic Mitigation Methodology, and Output PQ Options A Practical Discussion and Concept Overview
- An Intuitive Understanding of Electrical Harmonics FSE-MM-2026