VFD’s & Harmonic Mitigation in Modern Water/Wastewater Applications

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Introduction:

Process systems within the water/wastewater industry is increasingly dependent on variable speed drives (VFDs, ASDs and VSD’s) to control flow, pressure, and lift applications. Utilizing VFDs/ASDs for these processes can create systemic electrical harmonics (both current harmonic distortion and voltage harmonic distortion), systemic resonance conditions, and drive secondary circuit conditions such as reflective wave/ringing of the VFD output voltage. High dielectric stress due to the PWM output waveform, and common mode (P-N/G) high frequency noise can also occur, which can compromise secondary cable insulation and motor bearing integrity.

The purpose of this paper and presentation is to provide a fundamental understanding of VFD/ASD installation considerations, electrical harmonics, and review basic harmonic mitigation strategies that can assist with proper circuit design and engineering.

Section 1: Fundamentals of Electrical Harmonics & Introduction to IEEE519-2022

- Circuit challenges due to electrical harmonics.
- Key systemic relationships
- A quick IEEE519-2022 review

Section 2: VFD Construction Considerations and Line Side Harmonic Mitigation Considerations

- Typical VFD/ASD Topology
- DC Bus Capacitors
- AC Line Reactors and DC Link Inductors
- Typical Harmonic Mitigation Strategies
- Active Front End Drives and Higher Order Harmonics

Section 3: Specificational Notes for VFD

- Secondary Circuit Design to Prevent Resonance & Common Mode Noise
- Pulse Width Modulated Output of the Inverter is not Sinusoidal
- PWM and Voltage Distortion
- Common Mode Noise
- VFD Output Specification Considerations

Section 1: Fundamentals of Electrical Harmonics & Introduction to IEEE519-2022

Circuit Challenges Due to Electrical Harmonics.

Harmonics affect various network elements within a system in multiple ways. Whenever harmonic currents flow through equipment, several issues arise:

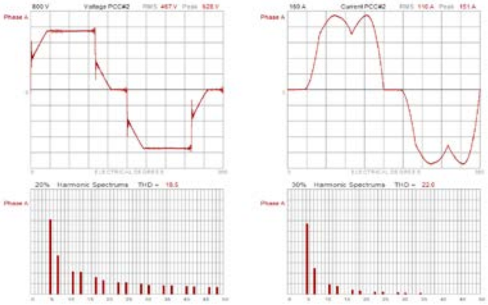
- Control & Protective Relay Nuisance Tripping: Harmonics can cause unintended tripping of relays and failure of capacitors installed for power factor improvement.
- Metering and Control Errors: Certain harmonic frequencies can have a reverse phase sequence, leading to incorrect readings in electro-mechanical metering devices. Additionally, elevated 24V DC

control bus ripple can compromise control and metering components.

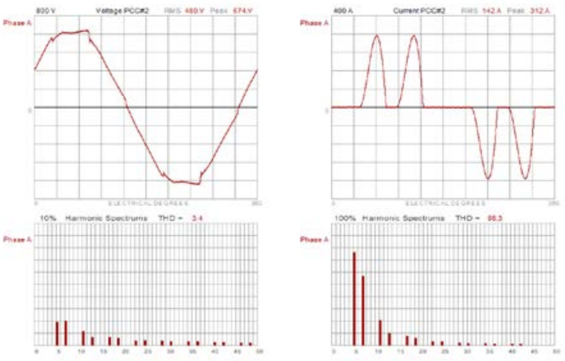
- Tele-Communication Interference: Higher order harmonics can interfere with telecommunication systems. When a communication line is parallel to a power line with harmonics present, noise may be introduced into the line, a phenomenon known as telephonic interference.
- Device Malfunction: Highly distorted voltage can cause malfunction in devices such as thyristors, diodes, and IGBT's. This is due to commutation errors and dielectric stress which can lead to component and assembly failures.
- True/Total Power Factor Reduction: High harmonic content will lower the true/total power factor of a system. TPF includes harmonic reactive power and is what the utilities measure, meaning TPF will be lower than displacement power factor (DPF)
- Increased Losses: Higher frequency current harmonics increase losses within equipment such as motors and transformers.
- Additional Cable Heating: Harmonic currents flow through the outer skin of conductors, resulting in additional conductor heating.
- Neutral Overheating: In a circuit with a neutral configuration, triplen harmonics tend to flow in the neutral. Many domestic and commercial non-linear loads generate a substantial amounts of 3rd order current harmonic. Third order harmonics can cause neutral conductors to overheat from excessive return path currents.
- Generator Challenges: Generators must be sized to accommodate incremental heating associated with harmonic load structures. The current harmonics associated with the non-linear loads will increase the eddy losses within the generator, significantly increasing the winding temperatures and stator losses. Harmonic mitigation strategies must include harmonic modeling of the traditional utility source and generator, if a generator backup source is present.

Fundamental Relationships of Electrical Harmonics

- Non-linear loads draw current in a non-sinusoidal manner, where the fundamental 60 Hz frequency is impacted by higher frequency current draws from the rectifier segment of the load device. Typically, we associate this with ASD/VFD applications, but it will exist in other diode bridge or IGBT rectifier loads such as UPS, DC rectifiers, and inductive heating systems to name a few.
- Drawing harmonic current then impacts the system voltage regulation, i.e. the instantaneous change in current negative and positive (di/dt) will create a corresponding change in the system voltage rate of change (dv/dt) of the source.
- Simply put, the injection of current harmonic into the system creates voltage distortion.
- The weaker the system, the greater the Vthd (Total Harmonic Distortion – Vthd) and the lower the Ithd (Total Harmonic Distortion – Current)



- The stiffer the system, the lower the Vthd (Total Harmonic Distortion) and the greater the Ithd (Total Harmonic Distortion – Current)



- Any linear load structure fed by a distorted source voltage will run less efficiently and draw current in a non-linear fashion, i.e., will now behave electrically as a non-linear load.
- A distorted voltage (Vthd) supplying a DC power supply can create additional DC bus ripple/distortion above the nominal amount, which has a significant impact on all control equipment being supplied by that DC source. This can then create issues for the LV DC components, sensors and transducers.
- High speed switching devices, such as IGBT based rectification or inverter applications will create supraharmonics. These current characteristics must be considered and evaluated within a credible harmonic review, modeling program, or testing protocol – typically between 2 kHz and 150 kHz.
- The greater the source voltage imbalance being provided to a non-linear load, the greater the impact to current harmonic (Ithd) and associated voltage distortion (Vthd) experienced.
- Current harmonics, non-work producing harmonic kVAR (Reactive Power), have a significant impact on the true/total power factor of the source.
- Power systems have a frequency band at which the inductive and capacitive elements are equal. Current harmonic frequencies that are drawn by non-linear loads within this band can result in resonance with the power system. The result of this harmonic resonance can be exhibited in the form of voltage reflective wave (Ringing), intermittent voltage transients, and elevated levels of source background voltage distortion.

Fundamentals of IEEE519-2022

IEEE519 was conceived and first introduced in 1981 as a recommended practice. The document included a write-up on the subject of electrical harmonics. The 2022 version is the third iteration and is now classified as a standard. Although the standard has undergone three revisions, the underlying principle and objective has remained unchanged. It defines acceptable levels of current and voltage harmonic to ensure a healthy power system. Below are key aspects to the IEEE519-2022 standard.

- IEEE519-2022 is a recommended standard.
- Two principal evaluation criteria are contained within the standard,
  ~ Table 1: Voltage Distortion Limit

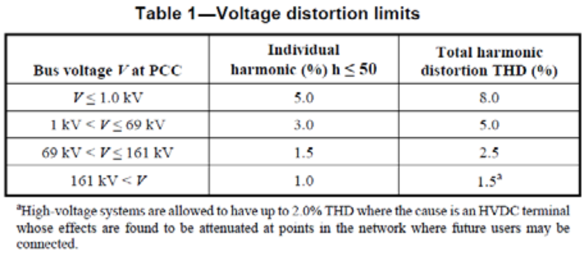


Table 1—Voltage distortion limits

Bus voltage V at PCC	Individual harmonic (%) $h \leq 50$	Total harmonic distortion THD (%)
$V \leq 1.0$ kV	5.0	8.0
1 kV < $V \leq 69$ kV	3.0	5.0
69 kV < $V \leq 161$ kV	1.5	2.5
161 kV < V	1.0	1.5^{a}

[a] High-voltage systems are allowed to have up to 2.0% THD where the cause is an HVDC terminal whose effects are found to be attenuated at points in the network where future users may be connected.

Note: The voltage distortion limits within Table 1 does not differentiate between source background voltage distortion and voltage distortion created by the current harmonic injection into the system impedance.

~ Table 2: Current Harmonic Limits

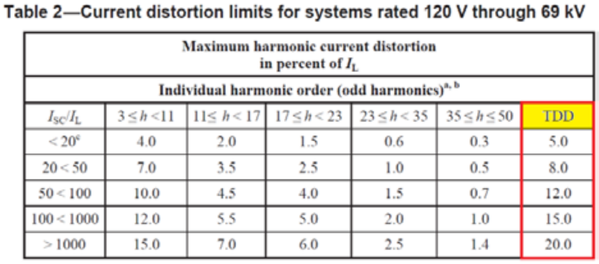
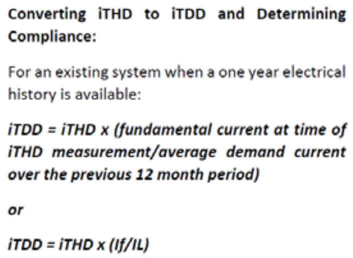


Table 2—Current distortion limits for systems rated 120 V through 69 kV

Maximum harmonic current distortion in percent of I_L						
Individual harmonic order (odd harmonics)[a, b]						
I_{SC}/I_L	$3 \leq h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h \leq 50$	TDD
< 20[c]	4.0	2.0	1.5	0.6	0.3	5.0
20 < 50	7.0	3.5	2.5	1.0	0.5	8.0
50 < 100	10.0	4.5	4.0	1.5	0.7	12.0
100 < 1000	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0



Converting iTHD to iTDD and Determining Compliance:

For an existing system when a one year electrical history is available:

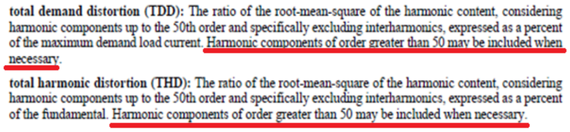
iTDD = iTHD x (fundamental current at time of iTHD measurement/average demand current over the previous 12 month period)

or

iTDD = iTHD x (If/IL)

- The standard is built on the principle that systemic voltage distortion limits – Table 1 can be met by following the current harmonic limits as prescribed in Table 2.

- Table 2 current harmonic limits are expressed as total demand distortion, not total harmonic distortion. See the summary conversion above, or consult published IEEE PCIC paper, Understanding the Relationship Between Total Harmonic Distortion and Total Demand Distortion in IEEE STD 519-2022: A Practical Discussion for Compliance Evaluation, PCIC 2024-58.
- The standard includes a full listing of definitions to standardize the vocabulary relative to the discussions of this topic. It also details the harmonic ranges that should be considered.



total demand distortion (TDD): The ratio of the root-mean-square of the harmonic content, considering harmonic components up to the 50th order and specifically excluding interharmonics, expressed as a percent of the maximum demand load current. Harmonic components of order greater than 50 may be included when necessary.

total harmonic distortion (THD): The ratio of the root-mean-square of the harmonic content, considering harmonic components up to the 50th order and specifically excluding interharmonics, expressed as a percent of the fundamental. Harmonic components of order greater than 50 may be included when necessary.

Section 2: VFD Topology and Harmonic Mitigation

- A variable frequency drive (VFD/ASD) takes an AC voltage, rectifies it, and then energizes a DC bus which functions as the source potential for the inverter. The inverter then creates a PWM voltage source waveform for the motor.
- The rectifier draws the current in pulses to charge the DC bus. This is the source of the current harmonic distortion drawn by the load. The injection of the current harmonic into the systemic impedance creates the associated voltage distortion.
- The DC bus will incorporate a DC bus capacitor which provides energy storage to reduce the amount of DC bus ripple. The DC bus capacitor also stiffens the source of the secondary circuit feeding the inverter.
- The output of the VFD is an inverter designed to switch the DC supply to create a pulse width modulated voltage waveform which approximates a sinusoidal wave through the RMS voltage values.
- The output waveform is not sinusoidal and has a high level of voltage distortion and dielectric stress due to the significant DV/DT associated with the PWM waveform. The function of the inverter will also create common mode noise (Phase to Ground/Neutral) partial discharge which can significantly impact the secondary circuit. This challenge is covered in section 3 of the paper.

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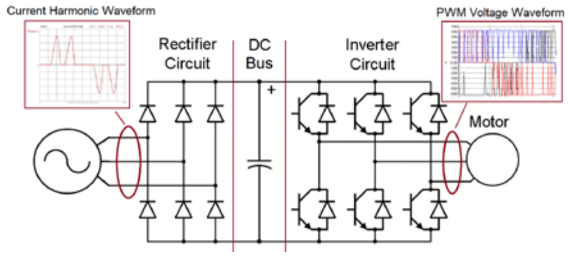
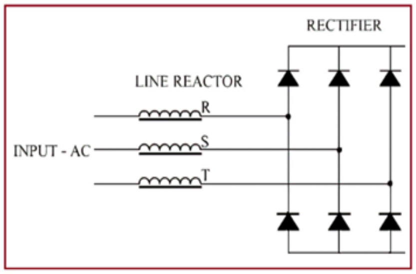


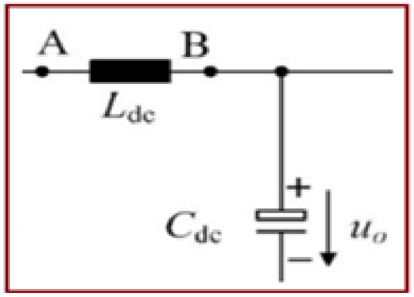
- A smaller DC bus capacitor reduces the VFD's physical size. However, it also reduces the stability of the DC bus voltage which weakens the DC bus source for the inverter output. This can create instability within the VFD itself due to:
  ~ Excess DC bus ripple which can impact the output PWM waveform.
  ~ Resonance between the DC bus capacitor and the upstream impedance/source and any reactive power sources upstream of the VFD.
  ~ Excess regulation and current imbalances due to the AVR (Automatic Voltage Regulation) modulation of the control circuit. The AVR setting of a VFD adjusts the sampling rate to compensate for the lower capacitance and provides protection from potential interactions with upstream impedances or to avoid excess DC bus ripple.

Other Common Options Which Can be Integrated into the VFD Assembly:

- AC Line Reactors:
  ~ The original concept of having an AC line reactor upstream of a drive was to add impedance thus ensuring the rectifier could withstand the source di/dt. Now, they are commonly used as a harmonic mitigation device, since a line reactor will lower the current harmonic associated with the VFD operation. Typically, it will lower the measured Ithd by around 50%.



- DC Link Inductors:
  ~ Adding impedance to the DC bus lowers the voltage ripple. A DC link inductor paired with a DC bus capacitor is often referred to as a DC bus filter. The reduction of the DC Bus ripple will lower the total harmonic current distortion of the VFD seen on the line side.



Active Front End Drives:

- AFE drives utilize an IGBT rectification scheme versus a diode bridge assembly. The concept is simple, by switching the rectifier at a higher speed, the lower order harmonics are reduced.
- Many manufacturers of AFE drives advertise that they comply with IEEE519-2022 but in fact do not when evaluated through the switching frequency range of the rectifier. Functionally, the current harmonic is shifted to a higher frequency band, typically around the switching speed of the rectifier. These higher

frequency harmonics are referred to as “Supraharmonics”.

- Higher order harmonics can have a significant impact on an electrical system. One major impact is to 24V DC control circuits by causing excess DC bus ripple.
- AFE Drives are susceptible to elevated levels of source/background voltage distortion and source voltage imbalances which can compromise their operation. Consult the manufacturer’s instruction book and application guide for details. If the source Vthd and source imbalance withstand is not covered within the instruction and applicational data, consult the manufacturer for the data.
- AFE VFD’s tend to be more expensive than traditional VFD’s utilizing passive filter harmonic mitigation or other forms of harmonic mitigation.
- Matrix technology drives are functionally different than an AFE drive, in that there is no DC bus assembly, where the rectifier and the inverter are a single assembly. This drive configuration generates a PWM output waveform to the motor without the need for rectification. The presence of higher order supraharmonics still exist within the operation and the same challenges for output circuit engineering are present as with a conventional active front end drive topology.

Typical Harmonic Mitigation Strategies

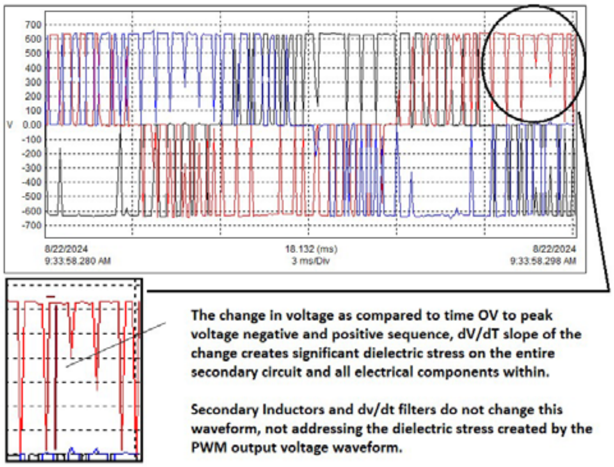
- Line Reactors & DC Inductors: Typically, this strategy only mitigates about 50% of the harmonic current content and does not comply with IEEE519 requirements.
- Multipulse Drives: In real world applications, multipulse drives (i.e. 18P Drives) utilizing an auto transformer for the phase shift are susceptible to elevated levels of source/ background voltage distortion and source voltage imbalances which can compromise their ability to meet IEEE519.
- Active Front End Drives: The introduction of supraharmonics (above the 50th harmonic – 3 kHz) may compromise compliance to IEEE519 requirements and introduce high frequency DC bus ripple in your control circuits within your circuit design.
- Passive Filters (LCL Config.): Passive filters offer higher versatility and reliability in a wider range of applicational/ source conditions. Passive filters are often the most cost effective solution as well. If a passive filter is selected for an application, care must be taken to specify two important criteria.
  ~ Compliance with IEEE519 requirements with up to 5% source Vthd and 3% source voltage imbalance.
  ~ To avoid over-excitation, the capacitance reactance to power ratio of the filter should not exceed 15% for designs of 100HP and up.

Section 3: Specificational Notes for VFD Secondary Circuit Design to Prevent Resonance & Common Mode Noise

Engineering a well-designed VFD secondary circuit is a combination of dielectric stress reduction, and the avoidance of reflective wave creation (ringing). Both conditions will compromise the life expectancy of the motor/load structure and can impact the inverter operation of the variable frequency drive.

Another key objective is to mitigate common mode noise (phase to ground) which can significantly compromise the motor/load via partial discharge across the bearing structures and can compromise the cable insultation due to phase to ground parasitic capacitance reactance. This condition can develop significant currents within the neutral and ground system, as well as induce ground and neutral voltage due to the resistance of the ground grid.

See Graphic 3-1 below for a wave-trace of a typical VFD output PWM waveform. What is shown is a repetitive zero to peak voltage sequence exposing the secondary circuit components, cabling, and motor to high dv/dt stress. This is typically referred to as differential noise and will lower the life cycle of the load structures unless the load components are built to an "Inverter Duty" specification. Inverter duty rated motors and shielded inverter duty rated cables are required when exposed to these voltage conditions. Inverter duty rated components are very expensive compared to standard cable and standard induction motors.

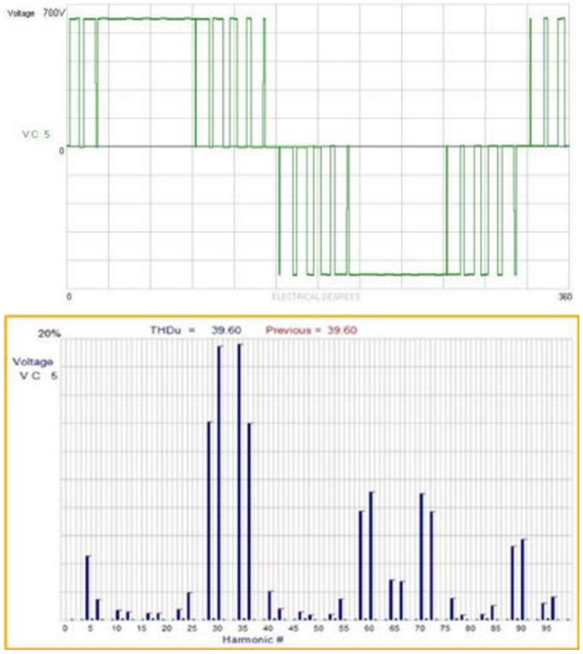


The change in voltage as compared to time OV to peak voltage negative and positive sequence, dV/dT slope of the change creates significant dielectric stress on the entire secondary circuit and all electrical components within.

Secondary Inductors and dv/dt filters do not change this waveform, not addressing the dielectric stress created by the PWM output voltage waveform.

Graphic 3-1

Secondary inductors and dv/dt filters do not change the functional dielectric stress within the system, they are simply attempting to "detune" the secondary circuit to avoid reflective wave, ringing, or resonance. They also do little to avoid Common Mode Noise applicational challenges.



Graphic 3-2

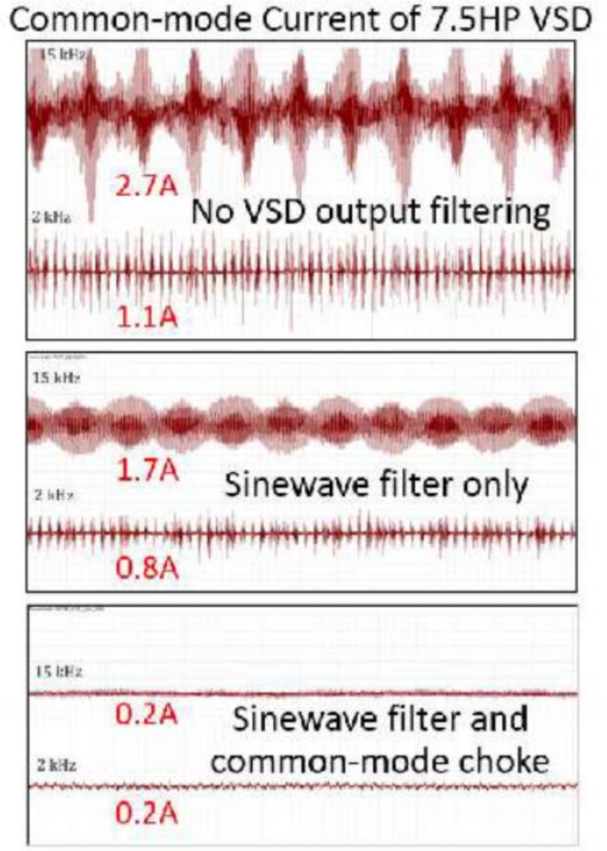
Above is the harmonic PWM output wave trace of an output inverter, with the associated harmonic spectrum. As is shown, the output voltage distortion is high and predominately at the switching frequency of the inverter, note the reflective harmonic band at integer intervals of the inverter switching frequency.

Common Mode Noise Challenge:

The damage from common mode noise within the secondary circuit is created by partial discharge across the motor bearings and associated mechanical load structures, and parasitic capacitance compromising cable insulation to the system ground. The graphic below 3-3 highlights common mode levels on a 7.5 HP VFD/VSD highlighting the substantial high frequency currents associated with common mode noise within the secondary circuit.

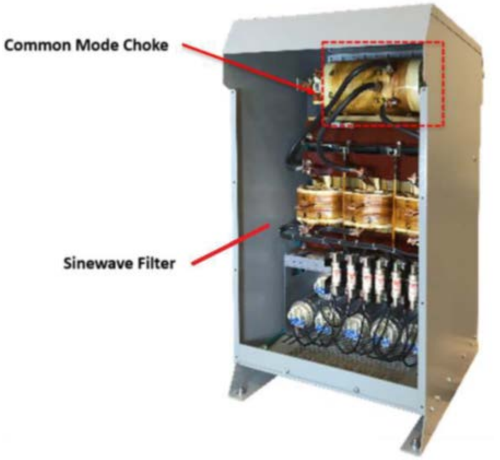
It also shows that a sinewave filter alone is not a viable solution for the common mode challenge. As the motor HP/ load increases, the associated CM noise current levels will increase significantly. The remedy to avoid premature motor and cable failures is to eliminate potentially destructive dielectric stress (dv/dt) by converting the PWM waveform to a sinusoidal waveform via a sinewave filter and utilizing a common mode choke.

This combination eliminates both differential and common mode dielectric stress associated with PWM inverter VFD/VSD secondary operations. In most cases, the cost of adding a sinewave filter and common mode choke is more than offset by the resulting savings from utilizing Standard unshielded cable and standard induction motors versus inverter duty rated components. In addition, a Mirus AUSF sinewave filter can increase the efficiency of the output circuit by 2% - 5% due to the elimination of eddy currents and secondary PWM losses by mitigating the voltage distortion of the PWM waveform.



Graphic 3-3

An estimated cost savings and payback analysis from utilizing a sinewave filter w/CMC can be found in Appendix A. This analysis includes the material savings from utilizing XHHW Type 2 cable with a standard induction motor versus an inverter duty rated motor and cable. Operating cost reduction from the resulting efficiency gains is also shown.



In summary, if you combine a sinewave filter and common mode choke into a single assembly/ solution, the customer/ user can avoid the need for shielded inverter duty rated cables and utilize standard Induction motors versus inverter duty rated motors, ultimately increasing the efficiency and life cycle of the secondary circuit.

Key Specificational Points: Clean Power VFD’s w/ Sinewave Filter & Common Mode Choke Assembly

- Output voltage waveform dV/dT stress and voltage overshoots characteristic for PWM inverter must be eliminated and suppressed without the need for snubber resistors, or auxiliary power electronic circuits.
- The sinewave filter shall have efficiency of no less than 99% and shall be suitable for application with PWM inverters that have carrier frequencies between 1.5 kHz to 8 kHz and motor leads up to 15,000 feet.
- The sinewave filter shall be tuned to 180 Hz versus 600Hz for differential noise mitigation of the 5th and 7th voltage

distortion frequencies to enhance efficiency of the secondary circuit. Total voltage distortion shall be <3% Vthd. The capacitive reactance of the sinewave filter at the load shall compensate for motor inductive reactive power such that power factor at the PWM inverter output is improved to 0.97 or better and will lower overall filter insertion loss (i.e. voltage drop) to < 3%.

- The sinewave filter cut-off frequency shall be set to approximately three (3) times the max allowed fundamental frequency of the PWM inverter to attenuate the carrier components at the rate of >40db per decade while minimizing the absorption of fundamental current by the filter.
- The sinewave filter shall eliminate the effects of reflected wave phenomenon. The need for VFD-rated cables and Inverter Duty Motors will be eliminated when the common-mode option is included.
- Inductors shall be air-gapped to control magnetic saturation. The inductance shall remain above 50% of its nominal value for any overload not exceeding 200% of rated current.
- Include common-mode choke option (CMC) to reduce the effects of common-mode currents on motor bearings and cable insulation.
- Option: Coordinated Surge Protection (CSP) with a minimum 100 kA withstand. The CSP option, when ordered, will provide a standard drive assembly 5 Year warranty.
- Integrated Drive Manufacturer Reference: Five Star Electric AS7 or AS100 CP-AUSF-CMC or equal approved prior to bid.

Technical References:

- IEEE/PCIC Paper PCIC-2010-15, Design Consideration When Applying Various ASD Topologies to Meet Harmonic Compliance.
- IEEE/PCIC Paper PCIC-2018-43, Active Harmonic Mitigation – What the Manufacturers Don't Tell You.
- A Practical Guide to Partial and Staged Harmonic Mitigation Strategies, MIRUS-TP006-A, Michael A McGraw, 05/12/2020
- The Need for Harmonic Modeling and Mitigation in Generator Applications Mike McGraw USA National Sales Manager, Mirus International Inc. Dated 06/24/2021
- An 'Intuitive Understanding' of Electrical Harmonics: A Conversation, Mike McGraw USA National Sales Manager, Mirus International Inc. Dated 03/08/2021
- Understanding the Relationship between Current Total Harmonic Distortion (Ithd)
- and Total Demand Distortion (TDD) in IEEE Std 519-2014, Group Paper - Mirus International Dated 03/30/2023
- Tutorial - Harmonic Challenges for Distribution Grid Design, 3 Hour IEEE Tutorial, IEEE/PES WNC Chapter, 03/05/2024
- FSE Document: FSE Output-TD001 2024/11/29: Specificational Notes for VFD Secondary Circuit Design to Prevent Resonance & Common Mode Noise
- FSE - Electrical Harmonics 101: An Overview of the Fundamentals of Electrical Harmonics and Discussion of Mitigation Strategies.
- FSE - Electrical Harmonics 102: A Further Review of Electrical Harmonics and Discussion of Mitigation Strategies with Discussion of VFD Secondary Circuit Design Considerations.

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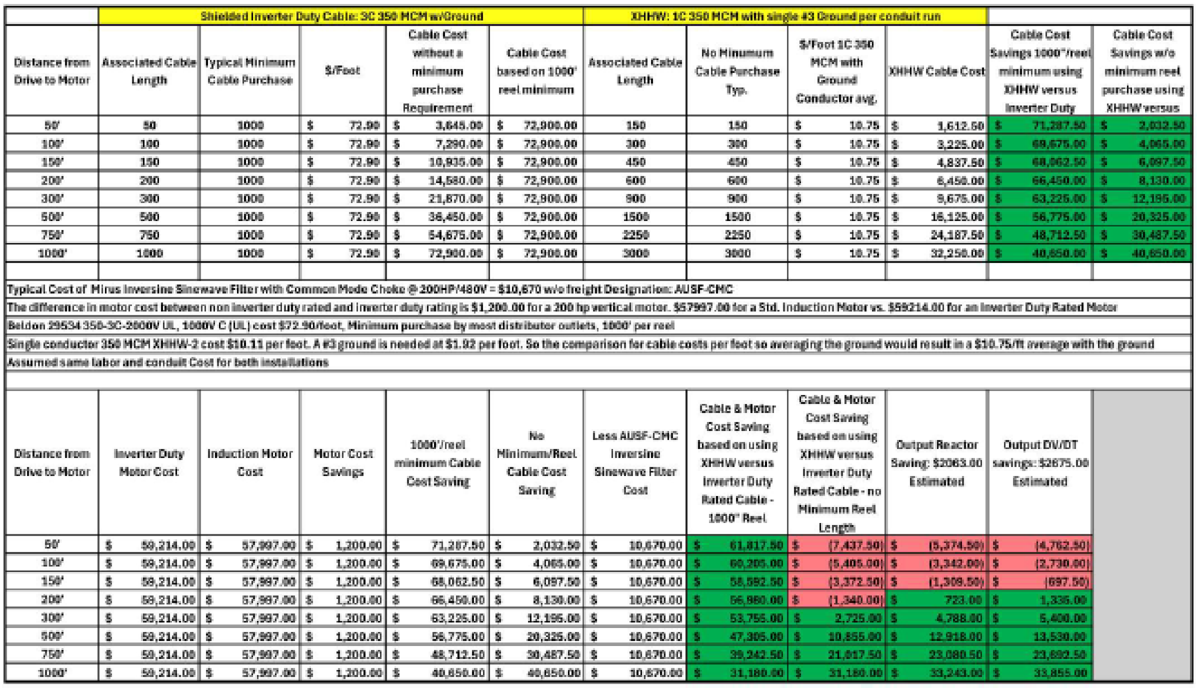
Austin Miller - Co-Author: currently serves as the Power Quality Sales Manager at Mirus International Inc., overseeing the U.S. market. Before joining Mirus International Inc. in 2023, he gained valuable experience as an application engineer specializing in power system harmonics at CTM Magnetics. He is a member of the IEEE.

Appendix A: Cost Payback Example 480V/200HP

- The typical minimum cable length purchase for Beldon Shielded Inverter Cable is 1000 foot, an analysis of both secondary circuit distance and a review of the cost of a 1000' cable reel length minimum purchase has been included. *<u>When considering a minimum cable reel length, under all distance considerations there is an immediate payback utilizing a Mirus AUSF-CMC filter saving significant project costs even up to 1000 cable lengths.</u>*
- If the AUSF-CMC filter is being utilized versus an inductor or dv/dt filter the immediate breakeven is just above 150' distance between the VFD and motor.



	Shielded Inverter Duty Cable: 3C 350 MCM w/Ground					XHHW: 1C 350 MCM with single #3 Ground per conduit run					
Distance from Drive to Motor	Associated Cable Length	Typical Minimum Cable Purchase	$/Foot	Cable Cost without a minimum purchase Requirement	Cable Cost based on 1000' reel minimum	Associated Cable Length	No Minumum Cable Purchase Typ.	$/Foot 1C 350 MCM with Ground Conductor avg.	XHHW Cable Cost	Cable Cost Savings 1000"/reel minimum using XHHW versus Inverter Duty	Cable Cost Savings w/o minimum reel purchase using XHHW versus
50'	50	1000	$ 72.90	$ 3,645.00	$ 72,900.00	150	150	$ 10.75	$ 1,612.50	$ 71,287.50	$ 2,032.50
100'	100	1000	$ 72.90	$ 7,290.00	$ 72,900.00	300	300	$ 10.75	$ 3,225.00	$ 69,675.00	$ 4,065.00
150'	150	1000	$ 72.90	$ 10,935.00	$ 72,900.00	450	450	$ 10.75	$ 4,837.50	$ 68,062.50	$ 6,097.50
200'	200	1000	$ 72.90	$ 14,580.00	$ 72,900.00	600	600	$ 10.75	$ 6,450.00	$ 66,450.00	$ 8,130.00
300'	300	1000	$ 72.90	$ 21,870.00	$ 72,900.00	900	900	$ 10.75	$ 9,675.00	$ 63,225.00	$ 12,195.00
500'	500	1000	$ 72.90	$ 36,450.00	$ 72,900.00	1500	1500	$ 10.75	$ 16,125.00	$ 56,775.00	$ 20,325.00
750'	750	1000	$ 72.90	$ 54,675.00	$ 72,900.00	2250	2250	$ 10.75	$ 24,187.50	$ 48,712.50	$ 30,487.50
1000'	1000	1000	$ 72.90	$ 72,900.00	$ 72,900.00	3000	3000	$ 10.75	$ 32,250.00	$ 40,650.00	$ 40,650.00

Typical Cost of Mirus Inversine Sinewave Filter with Common Mode Choke @ 200HP/480V = $10,670 w/o freight Designation: AUSF-CMC

The difference in motor cost between non inverter duty rated and inverter duty rating is $1,200.00 for a 200 hp vertical motor. $57997.00 for a Std. Induction Motor vs. $59214.00 for an Inverter Duty Rated Motor

Beldon 29534 350-3C-2000V UL, 1000V C (UL) cost $72.90/foot, Minimum purchase by most distributor outlets, 1000' per reel

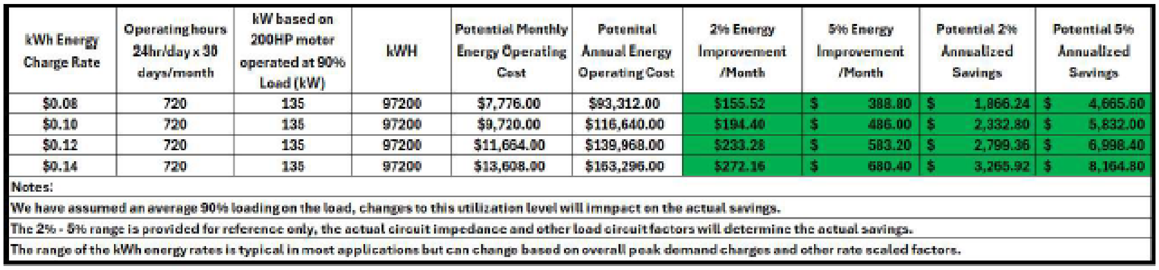
Single conductor 350 MCM XHHW-2 cost $10.11 per foot. A #3 ground is needed at $1.92 per foot. So the comparison for cable costs per foot so averaging the ground would result in a $10.75/ft average with the ground

Assumed same labor and conduit Cost for both installations

Distance from Drive to Motor	Inverter Duty Motor Cost	Induction Motor Cost	Motor Cost Savings	1000'/reel minimum Cable Cost Saving	No Minimum/Reel Cable Cost Saving	Less AUSF-CMC Inversine Sinewave Filter Cost	Cable & Motor Cost Saving based on using XHHW versus Inverter Duty Rated Cable - 1000" Reel	Cable & Motor Cost Saving based on using XHHW versus Inverter Duty Rated Cable - no Minimum Reel Length	Output Reactor Saving: $2063.00 Estimated	Output DV/DT savings: $2675.00 Estimated
50'	$ 59,214.00	$ 57,997.00	$ 1,200.00	$ 71,287.50	$ 2,032.50	$ 10,670.00	$ 61,817.50	$ (7,437.50)	$ (5,374.50)	$ (4,762.50)
100'	$ 59,214.00	$ 57,997.00	$ 1,200.00	$ 69,675.00	$ 4,065.00	$ 10,670.00	$ 60,205.00	$ (5,405.00)	$ (3,342.00)	$ (2,730.00)
150'	$ 59,214.00	$ 57,997.00	$ 1,200.00	$ 68,062.50	$ 6,097.50	$ 10,670.00	$ 58,592.50	$ (3,372.50)	$ (1,309.50)	$ (697.50)
200'	$ 59,214.00	$ 57,997.00	$ 1,200.00	$ 66,450.00	$ 8,130.00	$ 10,670.00	$ 56,980.00	$ (1,340.00)	$ 723.00	$ 1,335.00
300'	$ 59,214.00	$ 57,997.00	$ 1,200.00	$ 63,225.00	$ 12,195.00	$ 10,670.00	$ 53,755.00	$ 2,725.00	$ 4,788.00	$ 5,400.00
500'	$ 59,214.00	$ 57,997.00	$ 1,200.00	$ 56,775.00	$ 20,325.00	$ 10,670.00	$ 47,305.00	$ 10,855.00	$ 12,918.00	$ 13,530.00
750'	$ 59,214.00	$ 57,997.00	$ 1,200.00	$ 48,712.50	$ 30,487.50	$ 10,670.00	$ 39,242.50	$ 21,017.50	$ 23,080.50	$ 23,692.50
1000'	$ 59,214.00	$ 57,997.00	$ 1,200.00	$ 40,650.00	$ 40,650.00	$ 10,670.00	$ 31,180.00	$ 31,180.00	$ 33,243.00	$ 33,855.00

The key to the AUSF-CMC is the integrated Common Mode Choke, which other manufacturers do not normally offer due to cost considerations. To utilize the XHHW unshielded cable and Std. Induction Motors, you must mitigate both the differential mode noise and common mode noise to eliminate the dielectric stress and parasitic capacitance that will impact on the secondary circuit.

With considerations of additional efficiencies from the Sinusoidal waveform feeding the secondary circuit and motor load, there could be a efficiency improvement within the operation of the loads and an associated energy savings which can result in a 2% - 5% improvement. The schedule below highlights the additional energy savings payback on top of the payback noted below…



kWh Energy Charge Rate	Operating hours 24hr/day x 30 days/month	kW based on 200HP motor operated at 90% Load (kW)	kWH	Potential Monthly Energy Operating Cost	Potenital Annual Energy Operating Cost	2% Energy Improvement /Month	5% Energy Improvement /Month	Potential 2% Annualized Savings	Potential 5% Annualized Savings
$0.08	720	135	97200	$7,776.00	$93,312.00	$155.52	$ 388.80	$ 1,866.24	$ 4,665.60
$0.10	720	135	97200	$9,720.00	$116,640.00	$194.40	$ 486.00	$ 2,332.80	$ 5,832.00
$0.12	720	135	97200	$11,664.00	$139,968.00	$233.28	$ 583.20	$ 2,799.36	$ 6,998.40
$0.14	720	135	97200	$13,608.00	$163,296.00	$272.16	$ 680.40	$ 3,265.92	$ 8,164.80

Notes:

We have assumed an average 90% loading on the load, changes to this utilization level will immpact on the actual savings.

The 2% - 5% range is provided for reference only, the actual circuit impedance and other load circuit factors will determine the actual savings.

The range of the kWh energy rates is typical in most applications but can change based on overall peak demand charges and other rate scaled factors.

The potential energy saving enhances the payback of adding a Sinewave Filter w/ Common Mode Choke and additional future energy cost savings making this circuit design a prudent engineering requirement.